1. (Amended) A semiconductor package, comprising:

a lead frame having a first side and a second side, and formed with a die pad and a plurality of leads surrounding the die pad, wherein the leads are each defined into an inner lead, an outer lead and a middle portion positioned between the inner lead and the outer lead, and each of the middle portions extends outwardly at sides thereof to form protrusions;

a1

an encapsulant for encapsulating the lead frame with the outer leads being exposed, wherein a cavity is formed in the encapsulant for exposing the die pad and the inner leads on the first side of the lead frame, allowing a semiconductor chip and bonding wires to be received in the cavity;

the semiconductor chip mounted in the cavity on the die pad of the first side of the lead frame;

the plurality of bonding wires formed in the cavity for electrically connecting the semiconductor chip to the inner leads of the lead frame; and

a lid adhered onto the encapsulant for covering an opening of the cavity.

REMARKS

Claims 1-8 are pending in the application. Claims 5-8 have been withdrawn as being drawn to a non-elected invention. Claim 1 has been amended by the present amendment solely to overcome the claim objections. Specifically, claim 1 has been amended in the manner suggested by the Examiner. The amendments are fully supported by the specification as originally filed.

A Letter to Official Draftsman and a marked-up copy of FIG. 2 are attached hereto, where reference numeral 18 has been added to FIG. 2, thereby representing a gap between the die pad 11 and the plurality of leads 12 (see specification at page 5, last paragraph). Approval of the drawing correction is respectfully requested.

Applicants' invention is directed to a semiconductor package capable of preventing resin flashes. A lead frame acts as a chip carrier, the lead frame having a die pad and a plurality of leads surrounding the die pad. Each lead is divided into an inner lead, a middle portion, and an outer lead. A resin compound (i.e., encapsulant) encapsulates the lead frame, except for the outer leads, the encapsulant forming a cavity for exposing the die pad and inner leads, such that a semiconductor chip can be received in the cavity and mounted on the die pad. The semiconductor chip is electrically connected to the inner leads by a plurality of bonding wires.

As recited in claim 1, the middle portion of each lead extends outwardly at sides thereof to form protrusions, so as to reduce spacing between adjacent middle portions of the leads (see protrusions 1220 of each middle portion 122 in FIG. 2).

The above-described semiconductor package can yield significant benefits. During fabrication of the encapsulant, when the resin compound flows to the middle portions of the leads, the narrowed arrangement or reduced spacing between the leads slows down the resin flow and reduces the area available for the resin compound to flash (see specification at page 7, first full paragraph). This flash-preventing mechanism taught by Applicants is achieved through modification of the lead structure, thereby simplifying the manufacturing process and enabling cost savings to be achieved.

Claims 1 and 2 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 5,523,608 to Kitaoka et al. (hereinafter "Kitaoka") in view of U.S. Patent 6,315,465 to Mizue et al. (hereinafter "Mizue"). Claims 3 and 4 were rejected under 35 USC 103(a) as being unpatentable over Kitaoka in view of Mizue, and further in view of U.S. Patent 5,479,051 to Waki et al. These rejections are respectfully traversed, and for convenience are addressed together.

Neither Kitaoka nor Mizue, whether taken alone or in combination, teach or suggest a semiconductor package having the arrangement of leads recited in claim 1, or that is capable of preventing resin flash. In fact, Kitaoka and Mizue fail to teach or suggest a semiconductor package having a flash-preventing mechanism.

Kitaoka discloses a multi-chip semiconductor package incorporating a solid state image sensor and a peripheral IC, for reducing packaging area (see column 2, lines 14-17). With reference to FIG. 1, as cited in the Office Action, the peripheral IC 6 is mounted on a lower surface of an island 7 of the lead frame L and sealed by a molded resin block 8 (see column 3, lines 45-55). The solid state image sensor 1 is mounted on an upper surface of the island 7 and received within a cavity formed by the molded resin block 8 that is sealed by a transparent lid 11. Therefore, according to the invention of Kitaoka, both a solid state image sensor and a peripheral IC can be mounted in a single package, thereby reducing packaging area, and allowing "video equipment such as video cameras to be miniaturized" (see column 5, lines 1-7).

Kitaoka does not teach or suggest a flash-preventing mechanism having the lead arrangement recited in claim 1 of the Applicants' invention. Kitaoka does not teach or suggest middle portions of leads which extend outwardly to form protrusions. As stated in the Office Action: "Kitaoka et al. fail to disclose each of the middle portions extends outwardly at sides thereof to form protrusions" (Office Action, page 4).

Mizue fails to remedy the deficiencies of the Kitaoka reference. Specifically, Mizue fails to teach or suggest a plurality of leads having middle portions which extend outwardly to form protrusions for preventing resin flashes.

Mizue discloses an optical module of the dual inline package (DIP) type, for electrically connecting a wiring substrate and a lead frame without wire bonding. As shown in FIGS. 2-4, a lead frame 2 has a plurality of inner lead pins 8 and outer lead pins 10 respectively provided with

connecting portions 8a and 10a for connecting a wiring substrate 20 (see column 5, lines 24-25). Electrodes 20a of the wiring substrate 20 are attached to the connecting portions 8a and 10a to thereby electrically connect the wiring substrate 20 to the lead frame 2 without the use of bonding wires (see column 6, lines 41-52). An electronic circuit encapsulating portion 18, formed by an encapsulating resin, is used to encapsulate the wiring substrate 20 and connecting portions 8a and 10a, allowing the outer lead pins 10 to be exposed and project from the encapsulating portion 18 (see column 4, lines 47-49), and thereby "bend ... into a hook shape" to form the configuration illustrated in FIG. 1 (see column 6, lines 18-23).

Mizue fails to teach or suggest a semiconductor package having a plurality of leads surrounding a die pad, a semiconductor chip mounted in a cavity, and a plurality of bonding wires formed in the cavity for electrically connecting the semiconductor chip to the leads. Moreover, Mizue has no teaching or suggestion of the lead arrangement recited in claim 1 which can prevent resin flashes.

The exposed outer lead pins 10 in Mizue are **not** equivalent to the leads having middle portions that form protrusions according to the Applicants' claimed invention. Because the middle portions of the leads are encapsulated in the Applicants' invention, the resin compound flowing to the middle portions is slowed by the reduced spacing between the protrusions, thereby preventing the occurrence of resin flash.

In contrast, the outer leads pins 10 of Mizue, notwithstanding their protruding shape, are exposed outside and are **not** in contact with the encapsulant, and thus cannot control the flow speed of the encapsulating resin.

Even if Mizue were somehow combined with Kitaoka, it would not be possible to produce the Applicants' claimed invention, for at least the reasons discussed above. Even if the

outer lead pins 10 of Mizue were somehow incorporated into Kitaoka, the protrusions thereof are exposed outside the encapsulant, and are **not** capable of preventing resin flash.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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APPENDIX A:
VERSION WITH MARKINGS TO SHOW CHANGES MADE

The title has been canceled, and replaced with the following new title:

FLASH-PREVENTING SEMICONDUCTOR PACKAGE

IN THE CLAIMS

Claim 1 has been amended as follows:

1. (Amended) A semiconductor package, comprising:

a lead frame having a first side and a second side, and formed with a die pad and a plurality of leads surrounding the die pad, wherein the leads are each defined into an inner lead, an outer lead and a middle portion positioned between the inner lead and the outer lead, and each of the middle portions extends outwardly at sides thereof to form protrusions;

an encapsulant for encapsulating the lead frame with the outer leads being exposed, wherein a cavity is formed in the encapsulant for exposing the die pad and the inner leads on the first side of the lead frame, allowing a semiconductor chip and bonding wires to be received in the cavity;

[a] the semiconductor chip mounted in the cavity on the die pad of the first side of the lead frame;

[a] the plurality of bonding wires formed in the cavity for electrically connecting the semiconductor chip to the inner leads of the lead frame; and

a lid adhered onto the encapsulant for covering an opening of the cavity.